

HCK
HCSL output

HDK
LVDS output

HPK
PECL output

NON - PLL

Jitter
0.2 ps

SMD

2.5V

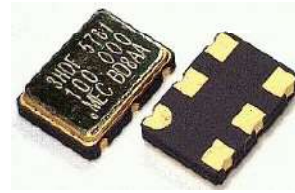
3.3V

Min.
40 MHz

Max.
200 MHz

Applications

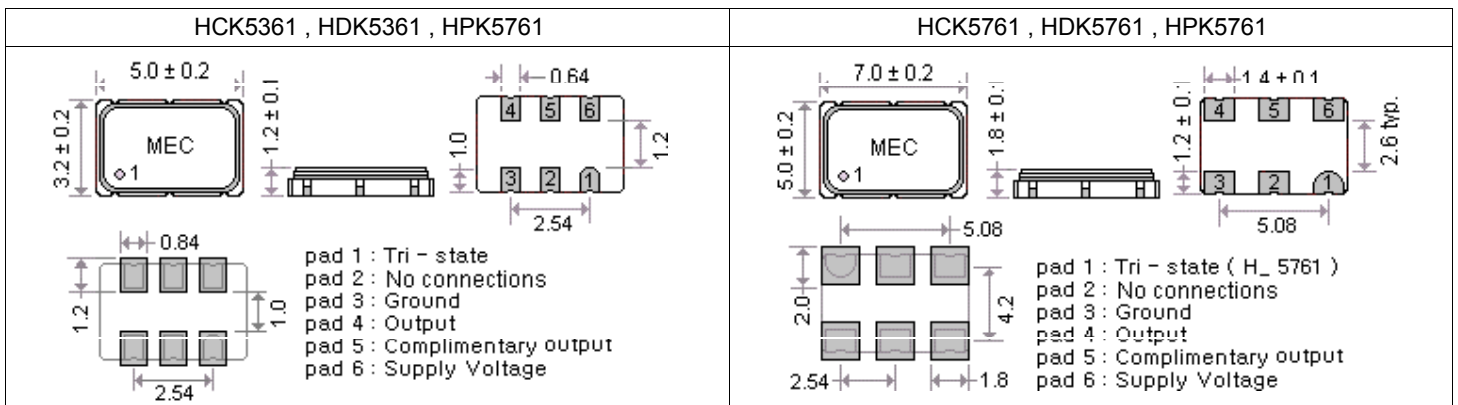
- Femto second integrated phase jitter (200 fs typical , 12 KHz to 20 MHz) .
- Superior phase noise (-138 dBc/Hz at 10 KHz and -144 dBc/Hz at 100 KHz offset)
- High performance with surprisingly low price .
- 2.5 V or 3.3 V supply voltage .



General specifications , at Ta=+25°C , CL=15pF

Model	HCK			HDK			HPK		
Output Logic	HCSL Differential			LVDS Differential			PECL Differential		
Available Frequency Range	10.0 MHz ~ 220.0 MHz			10.0 MHz ~ 220.0 MHz			10.0 MHz ~ 220.0 MHz		
Supply Voltage V _{DD}	+2.5 V _{DD} ± 5%	+3.3 V _{DD} ± 5%		+2.5 V _{DD} ± 5%	+3.3 V _{DD} ± 5%		+2.5 V _{DD} ± 5%	+3.3 V _{DD} ± 5%	
Supply Voltage Code	" 25 "	" 3 "		" 25 "	" 3 "		" 25 "	" 3 "	
Integrated Phase Jitter (12 KHz to 20 MHz)	0.2 ps typical ; For 155.520 MHz			0.2 ps typical ; For 155.520 MHz			0.2 ps typical ; For 155.520 MHz		
Output Logic " High " , " 1 " , V _{OH}	660 mV min. , 740 mV typ. , 850 mV max.			1.4 V typical ; 1.6 V max.			V _{DD} -1.025 min. V _{DD} -0.95 typ. V _{DD} -0.88 max.		
Output Logic " Low " , " 0 " , V _{OL}	-150 mV min. , 0 mV typ. , 150 mV max.			0.9 V typical ; 1.1 V max.			V _{DD} -1.810 min. V _{DD} -1.7 typ. V _{DD} -1.62 max.		
Output Voltage Swing	620 mV min. , 700 mV typ. , 780 mV max.			250 mV min. , 350 mV typ. , 450 mV max.			595 mV min. , 750 mV typ. , 930 mV max.		
Load	50 Ω to ground on each output			100 Ω between output and complimentary output			50 Ω into Vcc - 2V or Thevenin equivalent		
Current Consumption (15 pF load)	< 90 MHz: 17 mA typ. , 27 mA max 90.1 MHz ~ 160 MHz : 25 mA max. 160.1 MHz ~ 200 MHz : 30 mA max..			16 mA typical , 27 mA max.			35 mA typical , 50 mA max.		
Rise Time / Fall Time (RL=100 Ω , CL=10 pF)	0.15 ns typical , 0.4 ns max. (20%↔81% of the HCSL wave form)			0.2 ns typical , 0.4 ns max. (20%↔81% of the LVDS wave form)			0.3 ns typical , 0.5 ns max. (20%↔81% of the PECL wave form)		
SSB Phase Noise [dBc / Hz (typical)]	Offset	125.0 MHz	156.250 MHz	Offset	54.0 MHz	156.250 MHz	Offset	125.0 MHz	156.250 MHz
	10 Hz	-50	-50	10 Hz	-60	-55	10 Hz	-50	-50
	100 Hz	-82	-80	100 Hz	-90	-85	100 Hz	-82	-80
	1 KHz	-116	-115	1 KHz	-115	-118	1 KHz	-116	-115
	10 KHz	-138	-135	10 KHz	-130	-131	10 KHz	-138	-135
	100 KHz	-144	-142	100 KHz	-143	-142	100 KHz	-144	-142
	1 MHz	-149	-147	1 MHz	-142	-145	1 MHz	-149	-147
	10 MHz	-155	-152	10 MHz	-145	-151	10 MHz	-155	-152
Start-up Time	5 ms typical ; 10 m sec. (max.)								
Duty Cycle	50% ± 5%. Measured at 1.25V								
Storage Temperature	-55°C to + 105°C								
Aging at Ta = +25°C	± 3 ppm max. first year ; ± 2 ppm max. per year thereafter								
Frequency Stability ⁽¹⁾ Codes	Frequency Stability over Operating Temperature Range			± 25 ppm	± 50 ppm	± 100 ppm	If non-standard , please enter the desired stability after the " C " or " I " represents . For example : " C20 " ± 20 ppm over -10°C to +70°C ; " I20 " ± 20 ppm over -40°C to +85°C		
	Commercial (-10°C to +70°C)			A	B	C			
	Industrial (-40°C to +85°C)			D	E	F			
Tri - State Function. 5761 on pad No. 1 5762 on pad No. 2	No Connection	Differential output wave and complimentary wave form outputs .							
	Disable	Both outputs are disabled (high impedance) when the Tri-state pad is taken below 0.45*Vcc referenced to ground (threshold) Oscillator is always On . Only buffer stage is disabled . Disable current : 50 uA max. (at 0.0V) , Disable time : 10 ns (max.)							
	Enable	At disabled mode , both outputs are enabled when Tri-state pad is taken above 0.45*Vcc referenced to ground (threshold) ; Enable time : 10ns + one period of the output frequency (max.)							

Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs



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